

METHOD AND SYSTEM FOR ATTACHING MULTIPLE CLOCK SOURCES TO AN SDRAM MEMORY ARRAY

TECHNICAL FIELD

[0001] The present invention relates to computer board layout, and more particularly to a method and system for improving clock signal integrity in a board layout wherein there are multiple clock sources for a memory array.

BACKGROUND OF THE INVENTION

[0002] In many typical computer board (also, "motherboard") layouts, there is only one memory bus master, the processor. However, designs have advanced such that computer boards can include multiple possible memory bus masters. For example, board layouts such as those incorporating Intel® Xscale™ or Intel® StrongArm™ processors support a memory bus mastering scheme which allows for multiple bus masters. The multiple bus masters could comprise, for example, the processor, a "companion" chip of the processor, and a FPGA (Field Programmable Gate Array).

[0003] Clock topologies for memory arrays in computer board designs with only one memory bus master are typically configured to minimize or eliminate clock skew and jitter where possible. One aspect of minimizing skew and jitter involves using a single, centralized clock source for the memory. A further aspect of minimizing skew and jitter involves configuring the board layout to make trace lengths from the centralized clock source to individual memory modules substantially equal, so that clock signal propagation times to each module are substantially the same. Further, regulating feedback signals are provided to the clock source..

[0004] Accordingly, in order to conform to typical clock topologies, a clock topology for a system with multiple memory bus masters could appear as shown in Fig. 1. That is, a centralized clock source 100 could have inputs CLKIN0, CLKIN1 and CLKIN2 connected to clock signals CLKOUT_BM0, CLKOUT_BM1

and CLKOUT_BM2, respectively. Signals CLKOUT_BM0, CLKOUT_BM1 and CLKOUT_BM2 represent independent clock signals from each of a plurality of possible memory bus masters, each of which could read from or write to the system memory. In Fig. 1, a memory array is represented by SDRAM (synchronous dynamic random access memory) modules 101. Each of the possible bus masters could supply an independent clock driving signal to the array via CLKIN0, CLKIN1 or CLKIN2.

[0005] Signals MBGNT_BM0, MBGNT_BM1 and MBGNT_BM2, representing control signals from a memory bus arbiter, could further be input to the clock source 100 at inputs INSEL0, INSEL1 and INSEL2, respectively, to select which of the possible bus masters was to be given access to the memory array and drive clock signals to the array. Signals OUTPUT4, OUTPUT5 and OUTPUT6 of the clock source 100 could be connected to inputs CLKIN_BM0, CLKIN_BM1 and CLKIN_BM2, respectively, of each bus master, to provide a regulating feedback signal to each bus master.

[0006] The clock source 100 has multiple clock outputs, OUTPUT0-OUTPUT3, each of which drives the same clock signal (either CLKIN0, CLKIN1 or CLKIN2) via a point-to-point connection to a clock input (CLK) of each SDRAM module 101. Trace lengths from the clock source 100 to each SDRAM module 101 may be substantially equal so that signal propagation times to each SDRAM module are substantially the same. Further, the clock source 100 has an output signal, OUTPUT7, which is fed back as a regulating reference signal, REFIN.

[0007] Notwithstanding the advantages that could be realized by a layout as illustrated in Fig. 1 for a board with multiple memory bus masters, there are practical concerns which render such an implementation infeasible in many cases. For example, the need to provide a feedback input from the centralized clock source, as described above, for each bus master, would increase the complexity and cost of whatever logic was acting as the bus master.

[0008] Thus, instead of using a centralized clock source 100 with multiple clock outputs as shown in Fig. 1, a system with multiple memory bus masters

DETAILED DESCRIPTION

[0014] In embodiments of the invention, clock signals driven by multiple memory bus masters may be connected by transmission lines to a common node which is in turn connected to clock inputs of a memory array. An isolating circuit may be placed in the transmission line between each memory bus master and the common node. The isolating circuit may be controlled by memory bus arbitration signals to select one bus master to drive clock signals to the memory array, while selecting the transmission lines of the other bus masters for isolation from the common node, by introducing a high impedance between the transmission lines and the common node to eliminate signal corruption effects.

[0015] Fig. 2 shows one such possible embodiment. In Fig. 2, clock signals generated by three possible memory bus masters are shown: SA:SDCLK1, SA11:SDCLK1 and FPGA:SDCLK1. (It should be understood that these signal names, and signal names identified hereinafter, are arbitrary and given by way of example only to illustrate of the principles of the invention.) The memory bus masters corresponding to signals SA:SDCLK1, SA11:SDCLK1 and FPGA:SDCLK1 could be any kind of logic configured to drive signals to a memory bus, and having an independent clock source. For example, according to an embodiment of the invention, signals SA:SDCLK1, SA11:SDCLK1 and FPGA:SDCLK1 could correspond, respectively, to a processor, a "companion" chip of the processor, and a field programmable gate array (FPGA). However, there could be more than three possible bus masters, and the bus masters could be logic chips of different types from the examples given.

[0016] FETs (field effect transistors) 200, 201 and 202 and associated connections constitute one possible embodiment of an isolation circuit as described above. Each of the memory bus master clock signals is connected via a transmission line 205 to the source electrode of one of FETs 200, 201 and 202. More particularly, SA:SDCLK1 is connected to the source electrode of FET 200, SA11:SDCLK1 is connected to the source electrode of FET 201, and FPGA:SDCLK1 is connected to the source electrode of FET 202. The drain electrodes of each of FETs 200, 201 and 202 are connected to a common node

204. The common node 204, in turn, is connected to the clock inputs of each of the SDRAM modules 101. (It should be understood that, for convenience, Fig. 2 shows transmission lines 205 in a schematic representation. In actuality, the transmission lines 205 could be of significantly different lengths and approach the common node 204 from different directions, depending upon where the bus master generating the clock source was located in the board layout.)

[0017] Each of the memory bus master clock signals may be associated with a control signal from a memory bus arbiter. For example, SA:SDCLK1 may be associated with control signal SA:SDCLK1_MBGNT, SA11:SDCLK1 may be associated with control signal SA11:SDCLK1_MBGNT, and FPGA:SDCLK1 may be associated with control signal FPGA:SDCLK1_MBGNT. Control signals SA:SDCLK1_MBGNT, SA11:SDCLK1_MBGNT and FPGA:SDCLK1_MBGNT may be connected, respectively, to the gate electrodes of FETs 200, 201 and 202.

[0018] A memory bus arbiter (not shown) may drive signals SA:SDCLK1_MBGNT, SA11:SDCLK1_MBGNT and FPGA:SDCLK1_MBGNT, and thus may determine which of the possible bus masters will drive clock signals to the memory array represented by the SDRAM modules 101. The SA:SDCLK1_MBGNT, SA11:SDCLK1_MBGNT and FPGA:SDCLK1_MBGNT signals apply biasing voltages to the gate electrodes of the respective FETs they are connected to, to turn the FETs on and off as needed to select one bus master to drive clock signals to the array, while selecting the transmission lines of the other bus masters for isolation from the common node to preserve clock signal integrity.

[0019] For example, the memory bus arbiter could determine that the bus master corresponding to the clock signal SA:SDCLK1 was to be given access to the memory bus. In such a case, the memory bus arbiter could output a high value for control signal SA:SDCLK1_MBGNT, and low values for each of control signals SA11:SDCLK1_MBGNT and FPGA:SDCLK1_MBGNT. The high value for control signal SA:SDCLK1_MBGNT would cause FET 200 to conduct, allowing the bus master corresponding to clock signal SA:SDCLK1 to drive clock

[0024] Several embodiments of the present invention are specifically illustrated and described herein. However, it will be appreciated that modifications and variations of the present invention are covered by the above teachings and within the purview of the appended claims without departing from the spirit and intended scope of the invention.